01 Oct 2007

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Keyou Wang

Ying Cheng

Mariesa Crow
Missouri University of Science and Technology, crow@mst.edu

Recommended Citation

K. Wang et al., "Development of a FACTS Real-Time Hardware-in-the-Loop Simulation," *Proceedings of the 39th North American Power Symposium, NAPS '07 (2007, Las Cruces, NM)*, pp. 118-123, Institute of Electrical and Electronics Engineers (IEEE), Oct 2007.
The definitive version is available at https://doi.org/10.1109/NAPS.2007.4402297

Development of a FACTS Real-Time Hardware-in-the-Loop Simulation

Keyou Wang, Mariesa L. Crow, Ying Cheng
University of Missouri-Rolla

***Abstract*—This paper describes an approach to simulate the bulk power transmission system using hardware-in-the-loop (HIL) FACTS devices. The architecture of the HIL simulation is described and a DSP-PC-based UPFC device designed for HIL simulation is presented. The implementation of UPFC hardware, software and basic control are discussed. Experimental results are provided to support the proposed concept.**

I. Introduction

THE family of Flexible AC Transmission System (FACTS) devices holds considerable promise as future advanced power system controllers [1]. Unified power flow controllers (UPFCs) are hybrid FACTS devices that can control both active and reactive power flow on the line and bus voltage [1-2].

Grid control has historically been decentralized due mainly to geographic and regulatory constraints. UPFCs are good candidates for distributed power grid control methodologies. Before UPFCs can be implemented on a wide-scale basis, they must coordinate their actions with each other dynamically and rapidly in the event of a contingency; therefore, extensive verification of operation should be carried out.

Traditional software-based simulation has the disadvantage of being unable to exactly replicate real operational conditions. On the other side, a small laboratory power system is not capable of fully capturing the depth and breadth of large-scale power system dynamics. One way to bridge the gap between simulation and real conditions is to combine real-time simulation (RTS) and hardware-in-the-loop (HIL) [3].

II. FACTS Interaction Laboratory (FIL)

The FACTS Interaction Laboratory (FIL) based on HIL-RTS has been developed at the University of Missouri-Rolla for advanced FACTS/UPFC research [4]. A conceptualization of the FIL is shown in Fig. 1. A realistically sized power system is modeled in the real-time simulation engine using a commercial iHawk Xeon multiprocessor system from Concurrent Computer Corp. The simulation engine is interfaced via a "hardware-in-the-loop" mechanism to provide voltage and power flow information to the UPFC devices at their interconnection points. This approach allows the UPFCs to be easily relocated within the larger system and different controls to be tested.

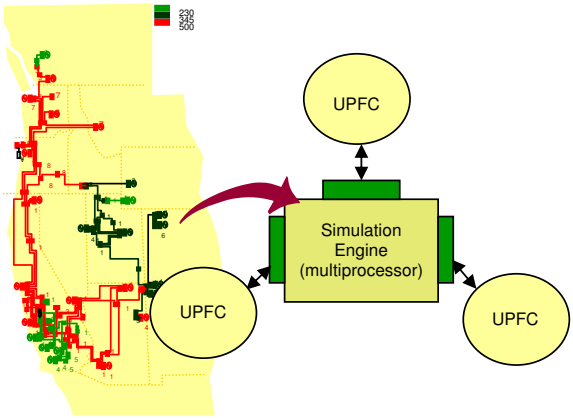

Fig. 1: The FACTS Interaction Laboratory Conceptualization

To date, three UPFC devices have been constructed. These devices are interconnected via the simulation engine that mimics the dynamic response of a power system. The simulation engine sends frequency, voltage, and current flow measurements to an external synchronous machine in the lab and a programmable load. The synchronous machine and programmable load generate the physical conditions that an actual UPFC device would encounter. The UPFC responds to these physical changes. The UPFC responses are fed back into the simulation as inputs. This setup is shown in Fig.2. The left portion of Fig.2 represents the simulation engine whereas the right portion shows the actual hardware. The synchronous machines are not part of the simulation but are used to produce the necessary active power flow on the lines in which the UPFC devices are placed. The programmable loads represent the load of the system "seen" by each of the UPFC devices. These loads change depending on the placement of the UPFC devices in the simulated power system.

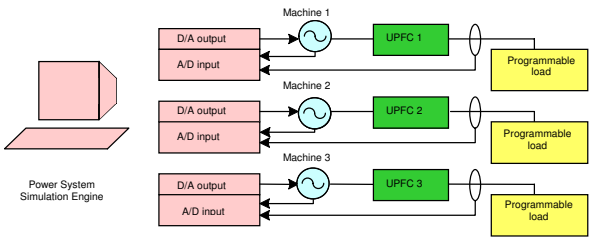

Fig.2. Conceptual layout of hardware and simulation engine

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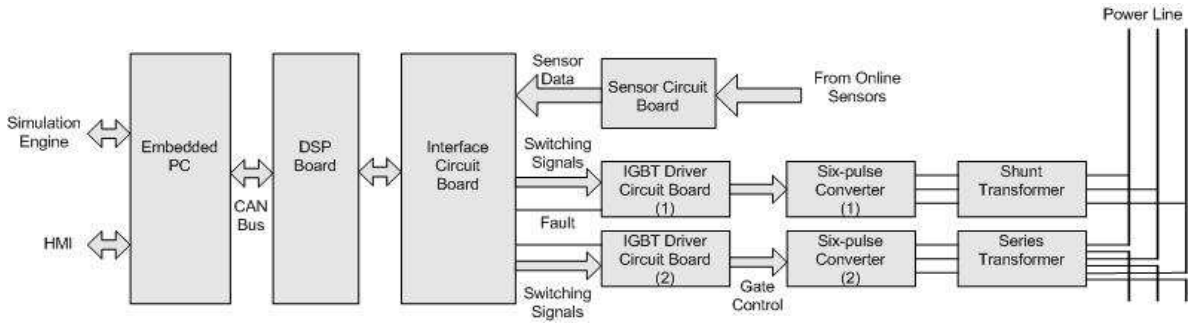

Fig. 3: Hardware architecture of a FACTS device

In the simulation, integration times are defined to be precisely the length of "real-world" time steps. Thus, the virtual dynamics of the larger system are meaningfully coupled to the physical hardware creating a real-time simulation. Synchronization with the physical world is done using real-time A/D (analog/digital) and D/A (digital/analog) I/O (input/output) boards.

III. Design of UPFC device

A. FACTS Overview

The FACTS/UPFC device is a laboratory scale PC-DSP-based real-time control system. This system makes use of hardware and software codesign to provide: 1) an accurate measurement system that can be used to perform fast and reliable signal processing; 2) enough power to implement the control algorithm and output the desired control digitals; 3) flexible communication interfaces for simulation engine and users [2].

Fig. 3 shows the hardware architecture of a FACTS/UPFC device. The design is comprised of three levels.

1) Power circuit level: two sets of three-phase Voltage-Source-Converters (VSC) and transformers.
2) DSP level: a MSK2812 Digital Signal Processing (DSP) board from Technosoft
3) PC level: a Linux based real time Embedded PC from Arcom

B. Power Circuit Level

The right portion of Fig. 3 represents the power circuit of UPFC device. It incorporates two voltage-source-converters (VSC) both in shunt (STATCOM) and in series (SSSC) with the transmission system. A capacitor is used to provide the dc voltage of the two back-to-back VSCs.

C. DSP Level

A TI TMS320F2812 DSP and peripheral hardware implement real-time data acquisition, CAN (Controller Area Network) bus communication with Embedded PC, SPWM control signal generation, synchronous function, and IGBT protection.

1) Data Acquisition

The main task of the data acquisition system is to acquire and preprocess up to 16 channels analog signals that are measured through voltage and current sensors from the FACTS device. Real-time signal processing such as digital filtering, phase calculation are also implemented in the DSP. The processed data (active and reactive power, RMS voltages, and currents) are exported to the embedded PC via CAN bus communication.

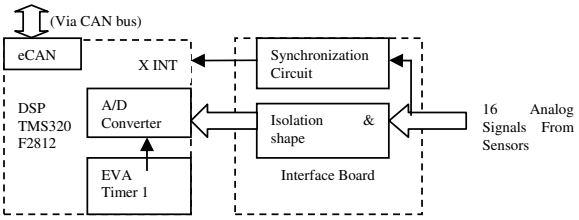

Fig. 4. Data Acquisition Hardware Configuration

The main hardware components of the data acquisition are shown in Fig. 4. The scaled analog data input channels from the external high power circuit are first isolated by ISO124 chips and the converted to digital signals. The shunt and series part each require eight input channels whereas the UPFC utilizes all 16 input channels. All of the analog data inputs are imported and stored in the DSP. The DSP on-chip timer is used to manage the data-acquisition sampling time.

2) SPWM signal generation

Sinusoidal pulse width modulation (SPWM) is used in this paper to generate switching signals. The DSP-based PWM control signal generation is capable of generating up to 12 programmable switching signals to the converters with adjustable dead time. For safety purposes, the FACTS device fault detection and protection are also accomplished.

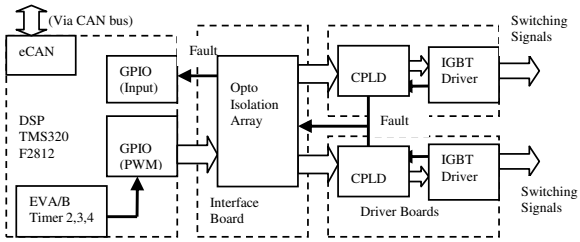

Fig. 5: SPWM signal generation hardware

The structure of the PWM signal generation hardware is shown in Fig. 5. The DSP will translate the updated control parameters such as modulation index and phase shift angle sent from embedded PC via CAN bus. Three DSP on-chip timers are used to manage the DSP on-chip PWM modules to generate 12-channel SPWM switching signals. The switching signals are firstly isolated in interface board and then sent to driver boards. Generally, the logic-level control signals are not powerful enough to directly switch the IGBTs; therefore, a Semkron IGBT driver module is used. The glue logic of fault signal detection, control button reaction from panel is implemented with a CPLD (Complex Programmable Logic Device) on the driver boards.

D. PC Level

The embedded PC is a linux-based real time system which provides FACTS dynamic control algorithm implementation and several access interfaces for users. The embedded PC communicates with the HIL simulation engine via TCP/IP network. It also has an independent Human Machine Interface (HMI) which provides data logging and online interaction to the control procedure.

The embedded PC receives the control target values from the HIL simulation engine or user interface input. The DSP exports the measured and processed data for control algorithm processing via the CAN bus. After controller calculation, the control variables (modulation ratio and phase shift) for the SPWM are sent back to the DSP via the CAN bus to generate switching signals. Since the control algorithm resides in the embedded PC, different control strategies can be programmed in C++ and implemented and modified rapidly.

E. UPFC control

The UPFC control algorithm proceeds by transforming the system measurements into a synchronous d-q reference frame and then using a PI compensator to regulate the converter ac-side currents and the dc-link voltage. The UPFC model in the d-q frame can be expressed as [2,5]

$$\frac{d}{dt}\begin{bmatrix} i_{pd} \\ i_{pq} \end{bmatrix} = \begin{bmatrix} -\frac{R_{s1}\omega_s}{L_{s1}} & \omega \\ -\omega & -\frac{R_{s1}\omega_s}{L_{s1}} \end{bmatrix} \begin{bmatrix} i_{pd} \\ i_{pq} \end{bmatrix} + \frac{\omega_s}{L_{s1}} \begin{bmatrix} E_{pd} - |V_s| \\ E_{pq} \end{bmatrix} \tag{1}$$

$$\frac{d}{dt}\begin{bmatrix} i_{sd} \\ i_{sq} \end{bmatrix} = \begin{bmatrix} -\frac{R_{s2}\omega_s}{L_{s2}} & \omega \\ -\omega & -\frac{R_{s2}\omega_s}{L_{s2}} \end{bmatrix} \begin{bmatrix} i_{sd} \\ i_{sq} \end{bmatrix} + \frac{\omega_s}{L_{ss}} \begin{bmatrix} E_{sd} + |V_s| - V_{rd} \\ E_{sq} - V_{rq} \end{bmatrix} \tag{2}$$

$$C\frac{dV_{dc}}{dt} = -\frac{1}{V_{dc}}(E_{pd}i_{pd} + E_{pq}i_{pq} + E_{sd}i_{sd} + E_{sq}i_{sq}) - \frac{V_{dc}}{R_{dc}} \tag{3}$$

where (1) represents the UPFC shunt part dynamics, (2) represents the UPFC series part dynamics, and (3) is the DC capacitor model, E_{pd} and E_{pq} are the shunt converter output voltages, and E_{sd} and E_{sq} are the series converter output voltages, which are expressed as

$$E_{pd} = 0.5k_1V_{dc}\cos\alpha_1, \quad E_{pq} = 0.5k_1V_{dc}\sin\alpha_1 \tag{4}$$

$$E_{sd} = 0.5k_2V_{dc}\cos\alpha_2, \quad E_{sq} = 0.5k_2V_{dc}\sin\alpha_2 \tag{5}$$

where k_1 and k_2 are the modulation index of the converters, and α_1 and α_2 are the phase angle between the converter output voltage and the synchronous reference voltage.

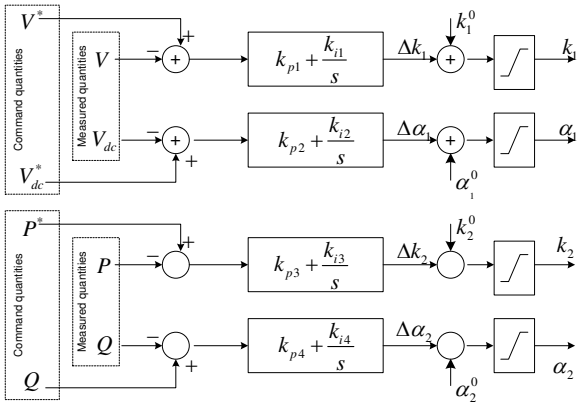

Fig. 6: UPFC control

Fig. 6 shows the basic PI control of the UPFC. The ac-bus voltage and dc-bus voltage can be maintained by controlling k_1 and α_1 of the UPFC shunt part; the active and reactive power flows can be maintained by controlling k_2 and α_2 of the series part.

IV. LAB EXPERIMENTS FOR FIL

Fig. 7 shows the laboratory setup for the simulation engine integrating a UPFC and the associated HIL line which includes an external synchronous machine and a programmable load (as illustrated in Fig. 2).

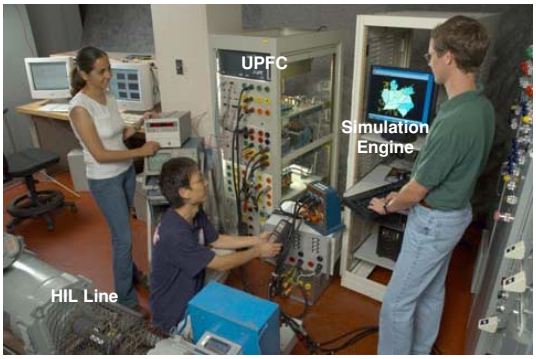

Fig. 7: Laboratory Setup

Fig. 8 shows a photograph of the UPFC which is constructed in the FIL with the following specifications:

- The ac line-line voltage is 115 volts at 60Hz.
- The dc voltage is 94 volts.
- The shunt part (STATCOM) is rated at 5kVA and the series part (SSSC) is rated at 6kVA.
- The line resistance is 1 Ω, the inductance is 16mH

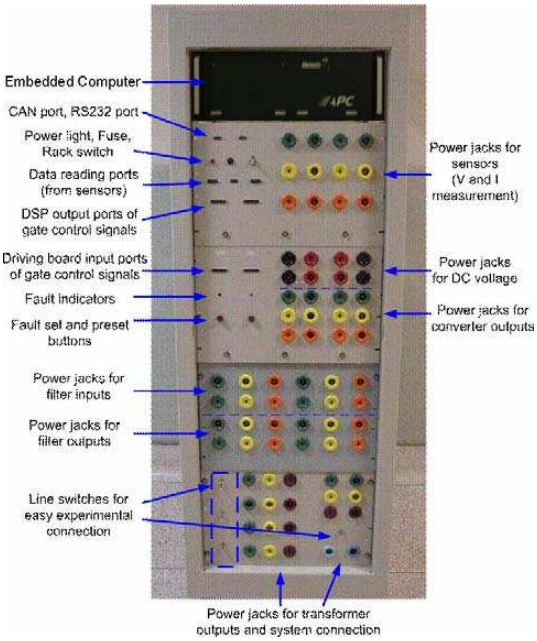

Fig. 8 photograph of the UPFC front panel

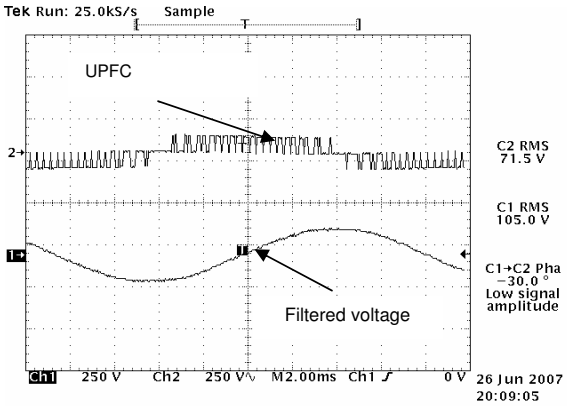

Fig. 9: Inverter line-line original voltage and filtered voltage

Fig. 9 shows the line-to-line shunt inverter output original voltage and filtered voltage. The LC filter is designed to eliminate the high order harmonics in the SPWM waveform.

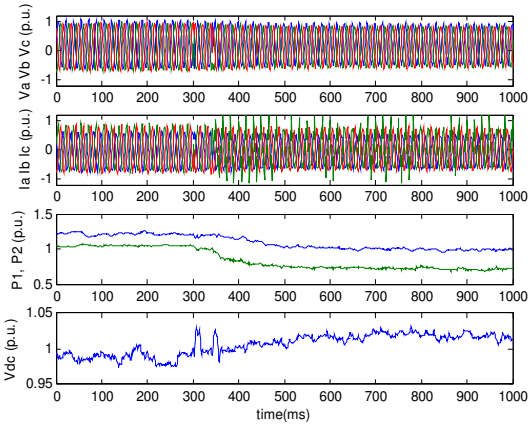

Fig. 10: Experimental results for active power step change

Fig. 10 shows the experimental results of an active power step change. In this experiment, the manual command to reduce the active power P from 1 to 0.75 p.u is sent via the HMI of embedded PC. The top two plots in Fig. 10 show the voltages and line currents. The third plot shows the sending end active power (P1 - blue) and the receiving end power (P2-green). The difference between P1 and P2 is due to the active power loss of the UPFC device. The dc capacitor voltage Vdc is controlled to maintain the constant value (1 p.u.).

Fig. 11 shows the lab result for manual power flow control. The top-left trace is the actual UPFC power flow in the HIL line. The top-right trace is the filtered power flow injected into the simulation engine. The bottom two traces show the simulated bus voltage and bus angle. This shows that the actual active power change is being successfully translated into the simulation and the simulated bus voltages and angles are responding appropriately.

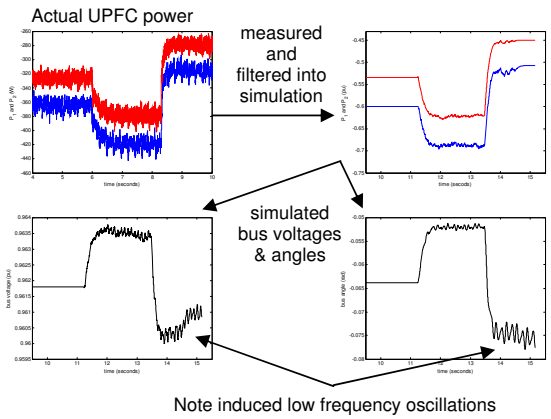

Fig. 11: Manual power flow control

V. Planned Experiments For the FIL

Fig. 12 shows the five different types of experiments (in yellow) that the FIL can perform. The other boxes indicate the kinds of theoretical developments that can be tested. The following are just a sample of the kinds of experiments that can be run:

1. different placements for up to three UPFCs for economic operation (steady-state) can be verified and tested. In this experiment, UPFCs can be placed in different places throughout the system and their steady-state active (and reactive) power flow control can be tested under changing load, generation, and line outages.
2. different types of dynamic UPFC control can be tested as well as the interaction between UPFCs and generators. Different placements can be validated.
3. the cyber-security and response of the system to a rogue UPFC can be tested and validated. Scenarios of intentional UPFC misbehavior can be studied and hardening schemes tested.

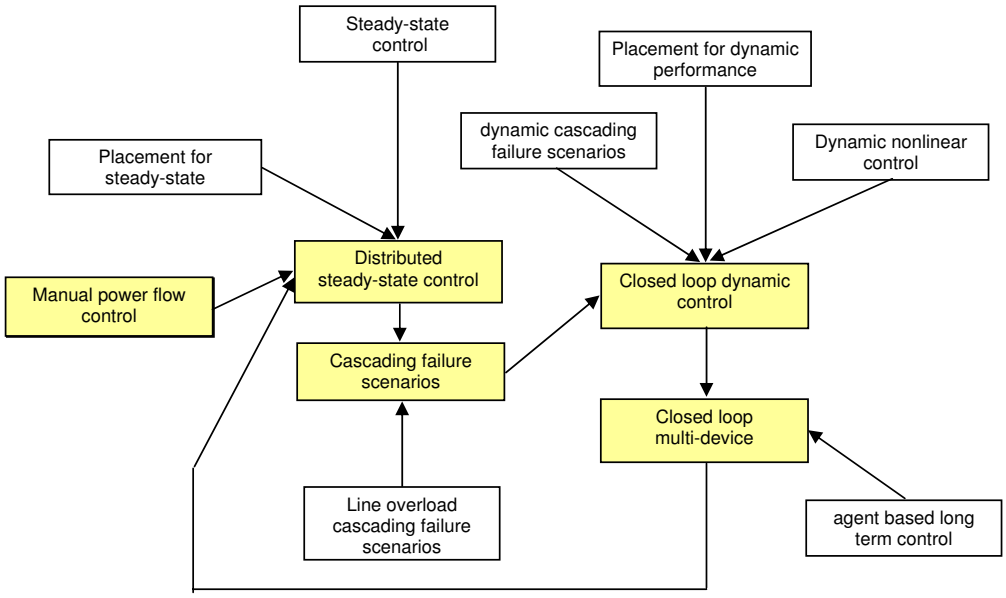

Fig. 12: Planned Experiments for FIL

VI. CONCLUSIONS

This paper describes an approach to simulate the bulk power transmission system using hardware-in-the-loop (HIL) FACTS devices. The architecture of the proposed system is described and a DSP-PC-based FACTS/UPFC device designed for HIL simulation is presented. The implementation of UPFC hardware, software and basic control are discussed. Preliminary experimental results show that the FACTS/UPFC device can meet the requirements of HIL simulation.

ACKNOWLEDGMENT

The authors gratefully acknowledge the support of the DOE Energy Storage Program, Sandia National Laboratories, and NSF CNS- 0420869 for this work.

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